WHAT IS CLAIMED IS:

1. A method of creating a compliant semiconductor chip package assembly comprising the steps of:

providing a first dielectric protective layer on a contact bearing surface of a semiconductor chip, wherein the semiconductor chip has a central region bounded by chip contacts of the semiconductor chip and wherein the dielectric protective layer has a plurality of apertures such that the chip contacts are exposed;

providing a compliant layer atop the first dielectric protective layer within the central region, wherein said compliant layer has a substantially flat top surface, a bottom surface that is attached to the first dielectric protective layer and sloping edges between the top surface and the bottom surface; and

selectively electroplating bond ribbons atop the first dielectric protective layer and the compliant layer wherein each bond ribbon electrically connects each chip contact to a respective conductive terminal on the top surface of the compliant layer.

2. The method according to Claim 1 further including the step of providing a second dielectric protective layer atop exposed assembly elements on the terminal side of the assembly after the step of selectively electroplating the bond ribbons, wherein the second dielectric protective layer has a plurality of apertures such that the terminals are exposed.

3. The method according to Claim 1 wherein the compliant layer material is selected from the group consisting of silicone, flexibilized epoxy, a thermosetting polymer, fluoropolymer, thermoplastic polymer, polyimide, foams and combinations or composites thereof.

4. The method according to Claim 1 further including the step of providing for an encapsulant layer atop ~~the~~ AN exposed surface of the bond ribbons.

5. The method according to Claim 4 wherein the encapsulant layer material is selected from the group consisting of silicone, flexibilized epoxy, thermoplastic and gel.

6. The method according to Claim 4 further including the step of providing for a second dielectric protective layer atop the encapsulant layer wherein the second dielectric protective layer has a plurality of apertures such that ~~the~~ terminal positions are exposed.

7. The method according to Claim 1 wherein a silicon dioxide passivation layer on the face surface of the semiconductor chip comprises the first dielectric protective layer.

8. The method according to Claim 1 further including the step of plating a barrier metal atop the semiconductor chip contacts, prior to the step of providing the compliant layer, whereby the barrier metal helps to prevent voiding at the boundary between the semiconductor chip contacts and the bond ribbons.

9. The method according to Claim 1 applied simultaneously to a multiplicity of undiced semiconductor chips on a wafer to form a corresponding multiplicity of compliant semiconductor chip packages, the method further including the step of dicing the packages following the step for selectively electroplating the bond ribbons.

10. The method according to Claim 1 applied simultaneously to a multiplicity of adjacent semiconductor chips arranged in an array to form a corresponding multiplicity of compliant semiconductor chip packages, the method further including the step of dicing the packages following the step for selectively electroplating the bond ribbons.

11. The method according to Claim 1 wherein the sloping edges of the compliant layer have a first transition region near the top surface of the compliant layer and a second transition region near the bottom surface of the

compliant layer and wherein both the first transition region and the second transition region have a radius of curvature.

12. A compliant semiconductor chip package assembly comprising:

a semiconductor chip having a plurality of peripheral chip contacts on a face surface thereof and a central region bound by the peripheral chip contacts;

a first dielectric protective layer having a first surface, a second surface and apertures, wherein the first surface of the first dielectric layer is attached to the face surface of the semiconductor chip and the apertures are aligned so that the chip contacts are exposed;

a compliant layer having a top surface, a bottom surface and sloping peripheral edges, wherein the bottom surface of the compliant layer is joined to the second surface of the first dielectric layer within the central region of the semiconductor chip package; and

a plurality of electrically conductive bond ribbons, each bond ribbon having a top surface, a bottom surface, a first end that electrically couples to a respective peripheral chip contact of the semiconductor chip, wherein each bond ribbon extends along the sloping edges to the top surface of the compliant layer and connects to a respective terminal.

13. The compliant semiconductor chip package of Claim 12 further including a second dielectric protective layer having a first surface that is attached to the exposed package assembly elements, wherein the second dielectric layer has a plurality of apertures such that the bonding pads of the semiconductor chip are exposed.

14. The compliant semiconductor chip package of Claim 12 further comprised of an encapsulant layer that is attached to the top surface of the bond ribbons.

15. The compliant semiconductor chip package of Claim 14 wherein the encapsulant layer material is selected from the group consisting of a curable liquid, silicone, flexibilized epoxy, thermoplastic and gel.

16. The compliant semiconductor chip package of Claim 12 wherein the plurality of package terminals are configured in an array having an area that is smaller than the area bound by the peripheral bonding pads on the face of the semiconductor chip.

17. The compliant semiconductor chip package of Claim 12, wherein the peripheral edge of the compliant layer has a first transition region near the top surface of the compliant layer and a second transition region near the second surface of the first dielectric protective layer and wherein the first and second transition regions have a radius of curvature.

18. The compliant semiconductor chip package of Claim 12, wherein the compliant layer material is selected from the group consisting of silicone, flexibilized epoxy, a thermosetting polymer, fluoropolymer, thermoplastic polymer and polyimide.

19. The compliant semiconductor chip package of Claim 12, wherein a plurality of bumped protrusions are provided and underly the plurality of package terminals such that an array of bumped package terminals is formed.

20. The compliant semiconductor chip package of Claim 12, wherein the top surface of the compliant layer has a plurality of concavities underlying the plurality of package terminals such that an array of concave-like package terminals is formed.